**Comparative study of the effects of coalesced and distributed solder die attach voids on thermal resistance of packaged semiconductor device**

<https://ieeexplore.ieee.org/abstract/document/6081033>

“thermal resistance increases more for large coalesced type voids in comparison to the small distributed void configurations”

“(Heat source) is applied as a heat flux on the top centre surface of the silicon chip with an area of 2mm×2mm (centre area)”





Good 2nd order approx. of 1/(1-v)+Ro

“For the same voiding percentage, lateral heat flow resistance is higher for large coalesced void patterns since the heat flows laterally for a much shorter distance for the small distributed voids. Thus, large coalesced voids result in a much more increase in the overall thermal resistance.”

Thermal characterization of die -attach degradation in the power MOSFET

<https://www.proquest.com/docview/305299133?pq-origsite=gscholar&fromopenview=true&sourcetype=Dissertations%20&%20Theses>

Void calc method (thresholding): “an error of about 5-10% is observed with this procedure” (P36)

**Transient Measurement of the Junction-To-Case Thermal Resistance Using Structure Functions: Chances and Limits**

<https://ieeexplore.ieee.org/abstract/document/4509389>

Shows limitations of structure function

<https://www.sciencedirect.com/science/article/pii/S1044580310000306>

shows how to do 3d void detection

<https://www.sciencedirect.com/science/article/pii/S0026271405002945#bib15>

Experimental measure of voids by location using controlled etching

VERY big difference of small vs big voids

Void dist algo: what is the average distance from a random pixel to the nearest non-void pixel? Also, do a weighted average where the pixel distances in the center are more important.